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inver$4 same data same (mask$3 adj1 (pin or terminal))	5

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inver$4 same data same (mask$3 adj1 (pin or terminal))	3

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L1	inver$4 same data same (mask$3 adj1 (pin or terminal))	5	L1

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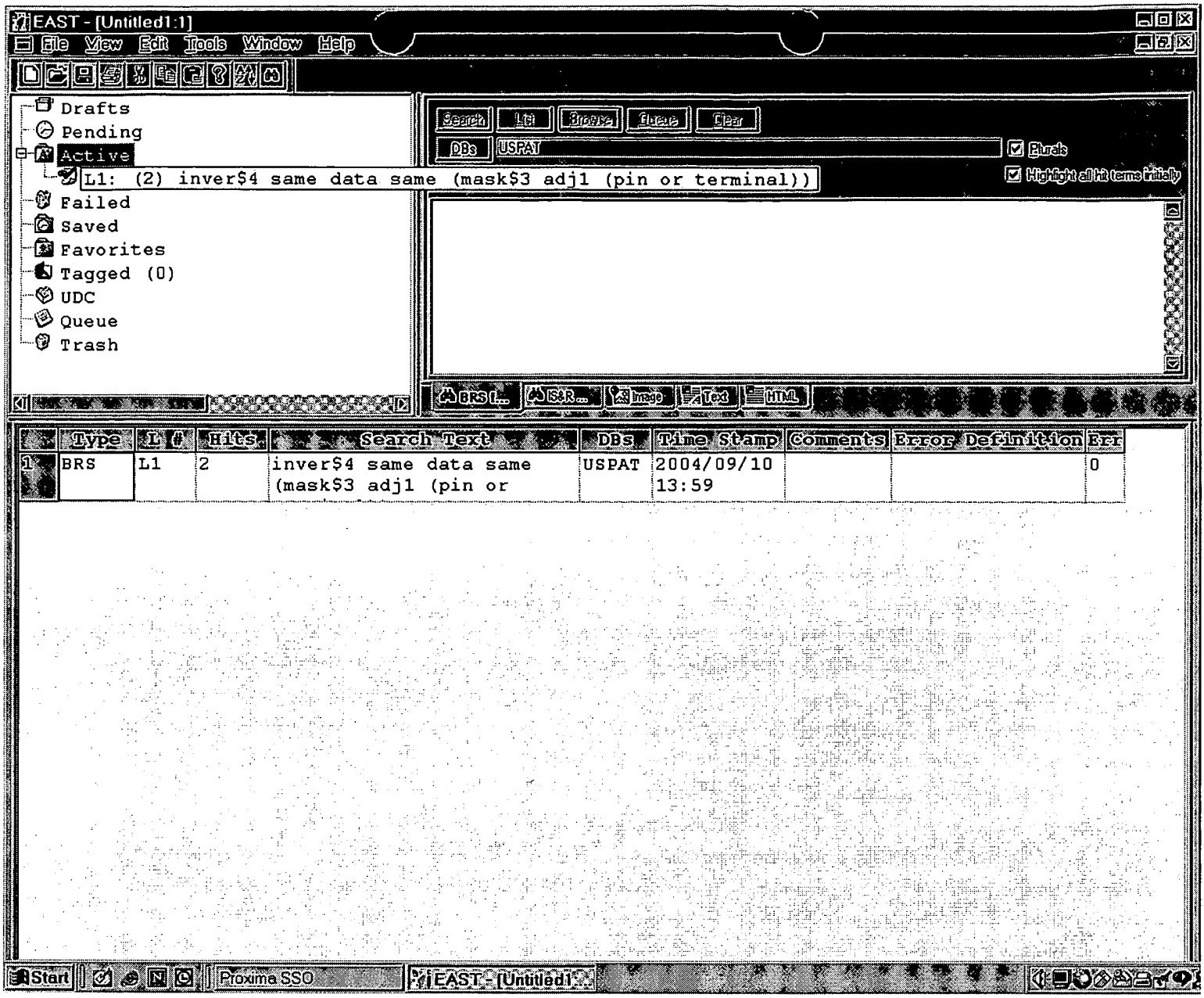
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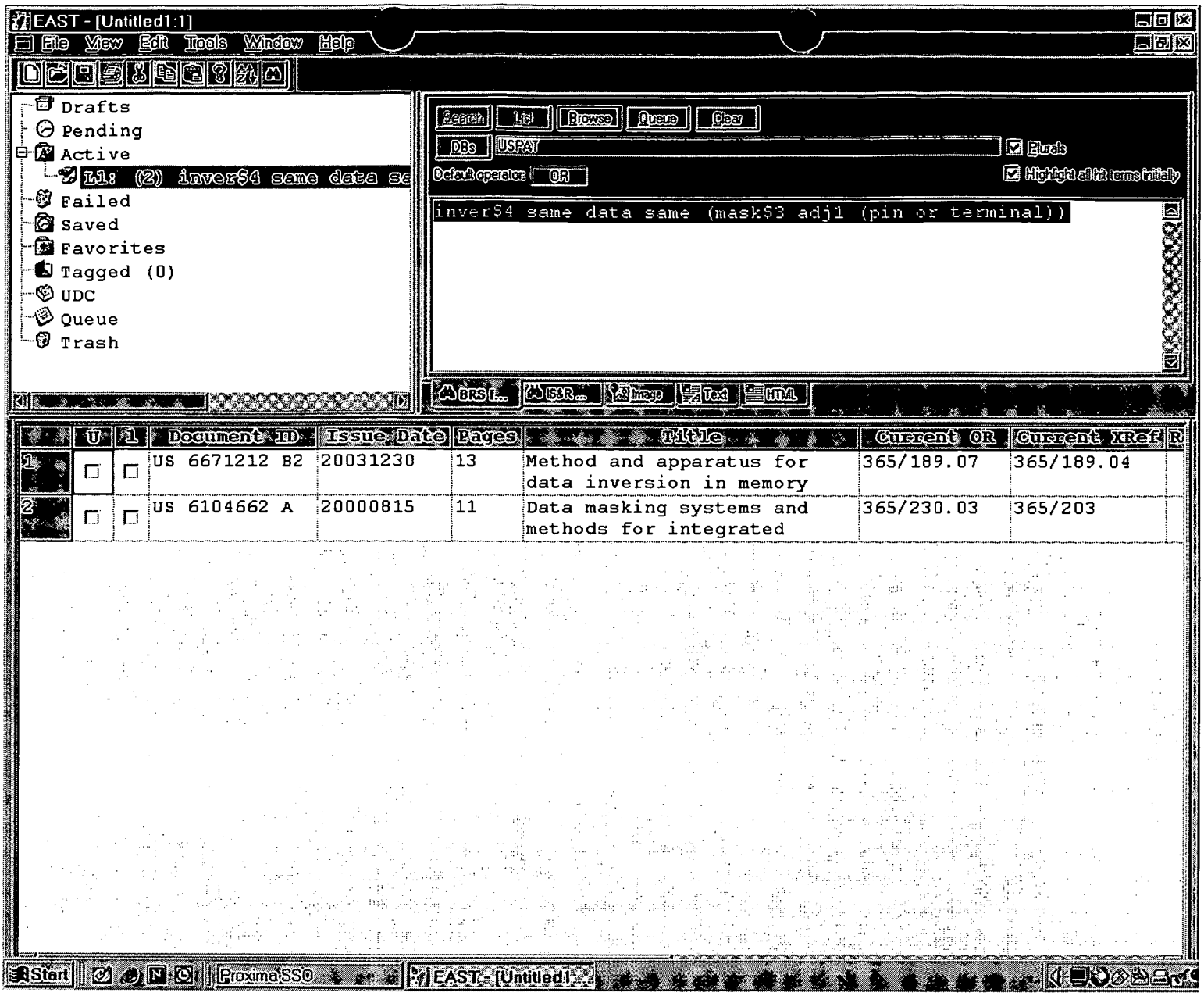
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JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

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1 **Monitoring detailed land surface changes using an airborne multisp digital camera system**
Stow, D.; Hope, A.; Nguyen, A.T.; Phinn, S.; Benkelman, C.A.;
Geoscience and Remote Sensing, IEEE Transactions on , Volume: 34 , Issue: 5 , Sept. 1996
Pages:1191 - 1203

[Abstract] [PDF Full-Text (1780 KB)] IEEE JNL

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2 **Reverberation characterization and suppression by means of princi components**
Palka, T.A.; Tufts, D.W.;
OCEANS '98 Conference Proceedings , Volume: 3 , 28 Sept.-1 Oct. 1998
Pages:1501 - 1506 vol.3

[Abstract] [PDF Full-Text (528 KB)] IEEE CNF

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3 **A linear inverse system approach in the context of chaotic communications**
Oksasoglu, A.; Akgui, T.;
Circuits and Systems I: Fundamental Theory and Applications, IEEE Transacti on [see also Circuits and Systems I: Regular Papers, IEEE Transactions on] , Volume: 44 , Issue: 1 , Jan. 1997
Pages:75 - 79

[Abstract] [PDF Full-Text (156 KB)] IEEE JNL

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4 **Auto-regressive estimation of spectral width of chirp sounder signa**
Salous, S.;
HF Radio Systems and Techniques, Seventh International Conference on (Cor

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Publ. No. 441) , 7-10 July 1997
Pages:115 - 119

[Abstract] [PDF Full-Text (436 KB)] **IEE CNF**

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5 **Inversion of modified beamformed array data**
Scheibner, D.; Parks, T.;
Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP '85. , Volume: 10 , Apr 1985
Pages:834 - 837

[Abstract] [PDF Full-Text (136 KB)] **IEEE CNF**

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6 **Lossless and lossy image compression using biorthogonal wavelet transforms with multiplierless operations**
HyungJun Kim; Li, C.C.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transacti
[see also Circuits and Systems II: Express Briefs, IEEE Transactions on] , Vol 45 , Issue: 8 , Aug. 1998
Pages:1113 - 1118

[Abstract] [PDF Full-Text (224 KB)] **IEEE JNL**

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7 **On the edge preserving smoothing filter**
Chih-Cheng Hung;
Southeastcon '97. 'Engineering new New Century'., Proceedings. IEEE , 12-1
1997
Pages:146 - 147

[Abstract] [PDF Full-Text (200 KB)] **IEEE CNF**

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8 **Data masking: a secure-covert channel paradigm**
Radhakrishnan, R.; Shanmugasundaram, K.; Memon, N.;
Multimedia Signal Processing, 2002 IEEE Workshop on , 9-11 Dec. 2002
Pages:339 - 342

[Abstract] [PDF Full-Text (354 KB)] **IEEE CNF**

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9 **Fusion of multi-frequency eddy current signals-by using wavelet an method**
Lingqi Li; Tsukada, K.; Hanasaki, K.; Zheng Liu;
Information Fusion, 2002. Proceedings of the Fifth International Conference on , Volume: 1 , 8-11 July 2002
Pages:108 - 113 vol.1

[Abstract] [PDF Full-Text (471 KB)] **IEEE CNF**

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10 **2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)**

Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on , Volume: 2 , 26-29 May 2002
[Abstract] [PDF Full-Text (9198 KB)] **IEEE CNF**

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11 **Evaluation of the MODIS vegetation index compositing algorithm u SeaWiFS data**
van Leeuwen, W.J.D.; Huete, A.R.; Laing, T.W.;
Geoscience and Remote Sensing Symposium Proceedings, 1998. IGARSS '98. IEEE International , Volume: 3 , 6-10 July 1998
Pages:1445 - 1447 vol.3

[Abstract] [PDF Full-Text (408 KB)] **IEEE CNF**

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12 **Optical signal processor for anti-counterfeiting and security systen**
Horner, J.L.; Javidi, B.;
Lasers and Electro-Optics Society Annual Meeting, 1994. LEOS '94 Conferenc Proceedings. IEEE , Volume: 1 , 31 Oct.-3 Nov. 1994
Pages:145 - 146 vol.1

[Abstract] [PDF Full-Text (184 KB)] **IEEE CNF**

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13 **A z-transform technique for thin-layer reverberation cancellation applied to ultrasonic NDT of adhered structures**
Freemantle, R.J.; Challis, R.E.; White, J.D.H.;
Advanced Techniques for Collection and Interpretation of NDT Data (Digest N 1994/102), IEE Colloquium on , 21 April 1994
Pages:7/1 - 7/4

[Abstract] [PDF Full-Text (216 KB)] **IEE CNF**

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14 **Integrated detectors for embedded optical interconnections on electrical boards, modules, and integrated circuits**
Sang-Yeon Cho; Sang-Woo Seo; Brooke, M.A.; Jokerst, N.M.;
Selected Topics in Quantum Electronics, IEEE Journal of , Volume: 8 , Issue: 6 , Nov.-Dec. 2002
Pages:1427 - 1434

[Abstract] [PDF Full-Text (538 KB)] **IEEE JNL**

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15 **Pulse compression for weather radars**
Mudukutore, A.S.; Chandrasekar, V.; Keeler, R.J.;
Geoscience and Remote Sensing, IEEE Transactions on , Volume: 36 , Issue: 1 , Jan. 1998
Pages:125 - 142

[Abstract] [PDF Full-Text (404 KB)] **IEEE JNL**

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Inversion of modified beamformed array data

Scheibner, D. Parks, T.
Rice University, Houston, Texas

This paper appears in: **Acoustics, Speech, and Signal Processing, IEEE International Conference on ICASSP '85.**

Publication Date: Apr 1985
On page(s): 834 - 837
Volume: 10

Abstract:
The separation of transient plane-waves as a function of their velocity and time-of-arrival can be performed by a time domain beamformer. Modifications in the beamformer output domain, such as **masking** out coherent interfering **signals** while taking into account both velocity and time information, are more straightforward than with traditional (k-ω) velocity filtering methods. We describe three methods of **inverting** the beamformer output to reconstruct the space-time samples. Of the three, one method, a block matrix **inversion** technique, is new. It is exact when operating on the original **data**, but fails when the beamformer output is modified. This problem can be alleviated by reducing the dimensionality of the **inversion** matrix using a singular value decomposition.

Index Terms:
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On the edge preserving smoothing filter

Chih-Cheng Hung
Dept. of Math. & Comput. Sci., Alabama A&M Univ., Normal, AL, USA;

This paper appears in: **Southeastcon '97. 'Engineering new New Century'., Proceedings. IEEE**

Meeting Date: 04/12/1997 - 04/14/1997
Publication Date: 12-14 April 1997
Location: Blacksburg, VA USA
On page(s): 146 - 147
Reference Cited: 8
Number of Pages: x+361
Inspec Accession Number: 5672505

Abstract:
An improvement on the gradient **inverse** weighted (GIW) filter for digital image smoothing is proposed. The selection of the optimal homogeneous neighboring pixels for spatial smoothing is achieved through the integration of directional **masks** and the adaptation of the selected subregion based on local statistics of the image **data**. This adaptive approach is effective in smoothing images containing complex-shaped objects such as remotely sensed imagery. Experimental results and the comparison with Tomita's (1977) filter, Nagao's (1979) filter, and the GIW filter are also presented

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Print Format

Index Terms:

adaptive filters adaptive **signal** processing edge detection image enhancement image segmentation nonlinear filters smoothing methods Nagao's filter Tomita's filter adaptive approach complex shaped objects digital image smoothing directional **masks** edge preserving smoothing filter experimental results gradient **inverse** weighted filter image **data** image enhancement local statistics nonlinear filtering algorithm optimal homogeneous neighboring pixels remotely sensed imagery spatial smoothing subregion adaptation

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L1: Entry 1 of 5 File: PGPB May 13, 2004

DOCUMENT-IDENTIFIER: US 20040090836 A1
TITLE: Method and apparatus for data inversion in memory device

Abstract Paragraph:
The present invention is a method of writing information to a synchronous memory device by examining a present word of N bits to be written, where each bit has a high or low value. The present word is compared to a previous word also having N bits to identify the number of bit transitions from a low value to a high value of vice versa. The present bit is inverted when the number of transitions is greater than N/2. To avoid the need for having an extra bit accompany data bytes to indicate the presence or absence of inversion, the present invention takes advantage of a data mask pin that is normally unused during writing operations to carry the inversion bit. Non-inverted data is written directly into the memory device while inverted data is first inverted again before writing to storage locations, so that true data is stored in the memory device.

Summary of Invention Paragraph:
[0010] The present invention is a method of writing information to a synchronous memory device by examining a present word of N bits to be written, where each bit has a high or low value. The present word is compared to a previous word also having N bits to identify the number of bit transitions from a low value to a high value of vice versa. The present bit is inverted when the number of transitions is greater than N/2. To avoid the need for having an extra bit accompany data bytes to indicate the presence or absence of inversion, the present invention takes advantage of a data mask pin that is normally unused during reading operations to carry the inversion bit. Non-inverted data is written directly into the memory device while inverted data is first inverted again before writing to storage locations, so that true data is stored in the memory device.

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L1: Entry 1 of 5 File: PGPB May 13, 2004

PGPUB-DOCUMENT-NUMBER: 20040090836
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20040090836 A1

TITLE: Method and apparatus for data inversion in memory device

PUBLICATION-DATE: May 13, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
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Drapkin, Olge	Richmond Hill		CA	
Temkine, Grigori	Markham		CA	
Nagashima, Osamu	Tokyo		JP	

APPL-NO: 10/ 681014 [PALM]
DATE FILED: October 7, 2003

RELATED-US-APPL-DATA:
Application 10/681014 is a continuation-of US application 10/163785, filed June 5, 2002, US Patent No. 6671212
Application is a non-provisional-of-provisional application 60/355289, filed February 8, 2002,

INT-CL: [07] G11 C 7/00

US-CL-PUBLISHED: 365/200
US-CL-CURRENT: 365/200

REPRESENTATIVE-FIGURES: 6

ABSTRACT:

The present invention is a method of writing information to a synchronous memory device by examining a present word of N bits to be written, where each bit has a high or low value. The present word is compared to a previous word also having N bits to identify the number of bit transitions from a low value to a high value of vice versa. The present bit is inverted when the number of transitions is greater than N/2. To avoid the need for having an extra bit accompany data bytes to indicate the presence or absence of inversion, the present invention takes advantage of a data mask pin that is normally unused during writing operations to carry the inversion bit. Non-inverted data is written directly into the memory device while inverted data is first inverted again before writing to storage locations, so that true data is stored in the memory device.

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L1: Entry 2 of 5 File: PGPB Aug 21, 2003

DOCUMENT-IDENTIFIER: US 20030158981 A1
TITLE: Memory bus polarity indicator system and method for reducing the affects of simultaneous switching outputs (SSO) on memory bus timing

Abstract Paragraph:
A method and system transfer read data from a memory device having a data bus and a data masking pin adapted to receive a masking signal during write operations of the memory device. The method includes placing a sequence of read data words on the data bus and applying a data bus inversion signal on the data masking pin, the data bus inversion signal indicating whether the data contained each read data word has been inverted. Another method and system transfer data over a data bus. The method includes generating a sequence of data words, at least one data word including data bus inversion data. The sequence of data words is applied on the data bus and is thereafter stored. The data bus inversion data is applied to invert or not invert the data contained in the stored data words.

Summary of Invention Paragraph:
[0012] According to one aspect of the present invention, a method and system transfer read data from a memory device having a data bus and a data masking pin adapted to receive a masking signal during write operations of the memory device. The method includes placing a sequence of read data words on the data bus and applying a data bus inversion signal on the data masking pin, the data bus inversion signal indicating whether the data contained each read data word has been inverted.

Brief Description of Drawings Paragraph:
[0016] FIG. 3 is a functional block diagram illustrating a memory system including a memory that supplies a data bus inversion signal to a memory controller over a data masking pin according to one embodiment of the present invention.

Detail Description Paragraph:
[0024] FIG. 3 is a functional block diagram illustrating a memory system 300 including a memory 302 that transfers data bus inversion information to a memory controller 304 over a data masking pin 306 of the memory during read data transfer operations. The memory 302 selectively outputs true or inverted read data words DQ1-N on a data bus DATA to minimize the switching of bits between consecutive read data words, and activates a data bus inversion signal DBI on the data masking pin 306 when inverted data is output and deactivates the DBI signal when true data is output, as will be explained in more detail below. The data masking pin 306 would normally be unused during read operations, but in the memory system 300 the memory 302 uses the data masking pin to apply the DBI signal to the memory controller 304 during read operations and in this way eliminates the need for additional dedicated pins on both the memory and memory controller, which reduces the costs of these devices. Moreover, the memory system 300 allows the memory 302 to transfer read data words DQ1-N to the memory controller 304 within specified timing parameters even as a width N of the data bus DATA increases since the transfer of true and inverted read data words minimizes the switching of bits in consecutive read data words and thereby reduces current required by the memory in driving the data bus, as will be discussed in more detail below. In the following description, certain details are set forth to provide a sufficient understanding of the present

invention. However, it will be clear to one skilled in the art that the present invention may be practiced without these particular details.

Detail Description Paragraph:
[0033] In the memory system 300, the memory 302 uses the data masking pin 306 of the memory during read operations to supply the DBI signal to the memory controller 304. In this way, an extra dedicated pin on the memory 302 for the DBI signal is not required which, as previously discussed, reduces the cost of memory modules containing a plurality of memories 302. The memory system 300 minimizes the switching of bits DQ1-N in consecutive read data words DW<1:N>, which reduces the current required by the read/write circuit 308 in driving the data bus and thereby reduces timing variations between data words and the DQS signal as more bits would otherwise change logic states between consecutive data words without the data bus inversion scheme of the memory system 300. In this way, the memory system 300 reduces the SSO pushout on the data bus DATA.

Detail Description Paragraph:
[0036] The transition detector 508 receives the NDW<1:N> word from the read latch 500 and the CDW<1:N> word output from the data driver 504 on the data bus DATA. The transition detector 508 determines the number of bits that change from a first logic state in the CDW<1:N> word to the complementary logic state in the NDW<1:N> word. When the detected number of bits is greater than N/2, the transition detector 508 activates the DBI signal on the data masking terminal 106 and deactivates the IC signal, turning OFF the pass gate circuit 506 and thereby causing the inverter circuit 502 to apply the NDW <1:N>* word to the input of the data driver 504. In contrast, when the detected number of bits is less than or equal to N/2, the transition detector 508 deactivates the DBI signal and activates the IC signal turning ON the pass gate circuit 506 and thereby applying the NDW <1:N> word to the input of the data driver 504.

Detail Description Paragraph:
[0037] In operation, assume an initial CDW <1:N> word has been latched by the data driver 504 and is initially being output on the data bus DATA. The read latch 500 thereafter latches the NDW <1:N> on the data path 116 in response to the ICLK1 signal, and outputs the latched word to the transition detector 508, pass gate circuit 506, and inverter circuit 502. At this point, the transition detector 508 compares the bits in the NDW<1:N> being output from the read latch 500 to the bits in the CDW <1:N> word currently being output by the data driver 504 on the data bus DATA. When the transition detector 508 determines number of bits changing from a first logic state in the CDW<1:N> word to the complementary logic state in the NDW<1:N> word is greater than N/2, the transition detector applies an active DBI signal on the data masking terminal 106 and deactivates the IC signal. In response to the deactivated IC signal, the pass gate circuit 506 turns OFF, causing the inverter circuit 502 to apply the NDW <1:N>* word to the input of the data driver 504. The ICLK2 signal thereafter clocks the data driver 504, causing the data driver to latch the NDW <1:N>* word and output this latched word as the CDW <1:N> word on the data bus DATA. In contrast, when the transition detector 508 determines number of bits changing from a first logic state in the CDW<1:N> word to the complementary logic state in the NDW<1:N> word is less than or equal to N/2, the transition detector applies an inactive DBI signal on the data masking terminal 106 and activates the IC signal. In response to the activated IC signal, the pass gate circuit 506 turns ON, causing the inverter circuit 502 to apply the NDW <1:N> word to the input of the data driver 504. The ICLK2 signal thereafter clocks the data driver 504, causing the data driver to latch the NDW <1:N> word and output this latched word as the CDW <1:N> word on the data bus DATA.

CLAIMS:

1. A method of transferring read data from a memory device, the memory device including a data bus and including at least one data masking pin adapted to receive

a data masking signal during write operations of the memory, the method comprising: placing a current read data word on the data bus, the read data word including a plurality of data signals and each data signal having a logic state; developing a next read data word, the next read data word including a plurality of data signals and each data signal having a logic state; comparing the logic state of each data signal in the current read data word to the logic state of the corresponding data signal in the next read data word; determining the number of data signals in the next read data word that are changing from a first logic state in the current read data word to the complementary logic state in the next read data word; when the determined number of data signals changing from the first logic state to the complementary logic state is greater than N, developing an inverted next read data word, each data signal in the inverted next read data word having a logic state that is the complementary logic state of the corresponding data signal in the next read data word, and activating a data bus inversion signal; placing the inverted next read data word on the data bus; and applying the activated data bus inversion signal on one of the data masking pins.

3. The method of claim 2 wherein the data bus includes X data signals, X being an integer multiple of 2N, and wherein a plurality of inverted next read data words are simultaneously applied on the data bus, each inverted next data word having an associated data bus inversion signal applied on an associated data masking pin.

5. A method of transferring read data from a memory device, the memory device including a data bus and including a data masking pin adapted to receive a masking signal during write operations of the memory device, the method comprising: placing a sequence of read data words on the data bus; and applying a data bus inversion signal on the data masking pin, the data bus inversion signal indicating whether the data contained each read data word has been inverted.

6. The method of claim 5 wherein the data bus inversion signal corresponds to a sequence of bits, each bit indicating whether a corresponding read data word in the sequence is to be inverted or not be inverted, and the bit associated with a particular read data word is applied on the data masking pin coincident with the particular read data word being placed on the data bus.

7. The method of claim 5 wherein each read data word includes a plurality of data bits, and wherein applying a data bus inversion signal on the data masking pin comprises: comparing the logic state of each data bit in a current read data word being placed on the data bus to the logic state of a corresponding data bit in a next read data word in the sequence that is to be placed on the data bus; determining the number of data bits in the next read data word that are changing from a first logic state in the current read data word to the complementary logic state in the next read data word; when the determined number of data bits changing from the first logic state to the complementary logic state is greater than N, developing an inverted next read data word, each data signal in the inverted next read data word having a logic state that is the complementary logic state of the corresponding data signal in the next read data word; activating the data bus inversion signal; and placing the inverted next read data word on the data bus and the activated data bus inversion signal on the data masking pin; and when the determined number of data bits changing from the first logic state to the complementary logic state is less than or equal to N, deactivating the data bus inversion signal; and placing the next read data word on the data bus and the deactivated data bus inversion signal on the data masking pin.

8. The method of claim 5 wherein the memory device includes a plurality of data masking pins, each read data word comprises 2N data bits, and the data bus includes X data bits where X is an integer multiple of 2N, and wherein a plurality of next read data words are simultaneously applied on the data bus, each next data word having an associated data bus inversion signal applied on an associated data masking pin.

16. A memory device, comprising: an address bus; a control bus; a data bus; an address decoder coupled to the address bus; a control circuit coupled to the control bus; a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; a data masking terminal adapted to receive a data masking signal during write operations of the memory device; and a read/write circuit coupled to the data bus, memory-cell array, and the data masking terminal, the read/write circuit operable during read operations to compare the number of bits changing from a first logic state in a current read data word on the data bus to the complementary logic state in a next read data word received from the memory-cell array, and operable in a first mode when the number of bits changing state is greater than a threshold value to apply an inverted next read data word on the data bus and apply an active a data bus inversion signal on the data masking terminal, and operable in a second mode when the number of bits changing state is less than or equal to the threshold value to apply the next read data word on the data bus and apply an inactive data bus inversion signal on the data masking terminal.

18. The memory device of claim 16 further comprising a plurality of data masking terminals and the read/write circuit operable to compare groups of bits in the current and next read data words, and to develop a corresponding data bus inversion signal for each group and apply each data bus inversion signal on a respective data masking terminal.

25. A computer system, comprising: a data input device; a data output device; a processor coupled to the data input and output devices; and a memory device coupled to the processor, the memory device comprising, an address bus; a control bus; a data bus; an address decoder coupled to the address bus; a control circuit coupled to the control bus; a memory-cell array coupled to the address decoder, control circuit, and read/write circuit; a data masking terminal adapted to receive a data masking signal during write operations of the memory device; and a read/write circuit coupled to the data bus, memory-cell array, and the data masking terminal, the read/write circuit operable during read operations to compare the number of bits changing from a first logic state in a current read data word on the data bus to the complementary logic state in a next read data word received from the memory-cell array, and operable in a first mode when the number of bits changing state is greater than a threshold value to apply an inverted next read data word on the data bus and apply an active a data bus inversion signal on the data masking terminal, and operable in a second mode when the number of bits changing state is less than or equal to the threshold value to apply the next read data word on the data bus and apply an inactive data bus inversion signal on the data masking terminal.

27. The computer system of claim 25 further comprising a plurality of data masking terminals and the read/write circuit operable to compare groups of bits in the current and next read data words, and to develop a corresponding data bus inversion signal for each group and apply each data bus inversion signal on a respective data masking terminal.

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L1: Entry 2 of 5 File: PGPB Aug 21, 2003

PGPUB-DOCUMENT-NUMBER: 20030158981
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030158981 A1

TITLE: Memory bus polarity indicator system and method for reducing the affects of simultaneous switching outputs (SSO) on memory bus timing

PUBLICATION-DATE: August 21, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
LaBerge, Paul A.	Shoreview	MN	US	

APPL-NO: 10/ 081652 [PALM]
DATE FILED: February 21, 2002

INT-CL: [07] G06 F 13/00

US-CL-PUBLISHED: 710/100
US-CL-CURRENT: 710/100

REPRESENTATIVE-FIGURES: 3

ABSTRACT:

A method and system transfer read data from a memory device having a data bus and a data masking pin adapted to receive a masking signal during write operations of the memory device. The method includes placing a sequence of read data words on the data bus and applying a data bus inversion signal on the data masking pin, the data bus inversion signal indicating whether the data contained each read data word has been inverted. Another method and system transfer data over a data bus. The method includes generating a sequence of data words, at least one data word including data bus inversion data. The sequence of data words is applied on the data bus and is thereafter stored. The data bus inversion data is applied to invert or not invert the data contained in the stored data words.

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L1: Entry 3 of 5 File: PGPB Aug 14, 2003

PGPUB-DOCUMENT-NUMBER: 20030151953
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030151953 A1

TITLE: METHOD AND APPARATUS FOR DATA INVERSION IN MEMORY DEVICE

PUBLICATION-DATE: August 14, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Macri, Joseph	San Francisco	CA	US	
Drapkin, Olge	Richmond Hill		CA	
Temkine, Grigori	Markham		CA	
Nagashima, Osamu	Tokyo		JP	

APPL-NO: 10/ 163785 [PALM]
DATE FILED: June 5, 2002

RELATED-US-APPL-DATA:
Application is a non-provisional-of-provisional application 60/355289, filed February 8, 2002,

INT-CL: [07] G11 C 5/00

US-CL-PUBLISHED: 365/189.01; 365/189.07
US-CL-CURRENT: 365/189.01; 365/189.07

REPRESENTATIVE-FIGURES: 1

ABSTRACT:

The present invention is a method of writing information to a synchronous memory device by examining a present word of N bits to be written, where each bit has a high or low value. The present word is compared to a previous word also having N bits to identify the number of bit transitions from a low value to a high value of vice versa. The present bit is inverted when the number of transitions is greater than N/2. To avoid the need for having an extra bit accompany data bytes to indicate the presence or absence of inversion, the present invention takes advantage of a data mask pin that is normally unused during writing operations to carry the inversion bit. Non-inverted data is written directly into the memory device while inverted data is first inverted again before writing to storage locations, so that true data is stored in the memory device.

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L1: Entry 4 of 5 File: USPT Dec 30, 2003

US-PAT-NO: 6671212
DOCUMENT-IDENTIFIER: US 6671212 B2

TITLE: Method and apparatus for data inversion in memory device

DATE-ISSUED: December 30, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Macri; Joseph	San Francisco	CA		
Drapkin; Olge	Richmond Hill			CA
Temkine; Grigori	Markham			CA
Nagashima; Osamu	Hamura			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
ATI Technologies Inc.	Markham			CA	03

APPL-NO: 10/ 163785 [PALM]
DATE FILED: June 5, 2002

PARENT-CASE:
This application claims the benefit of Provisional application Ser. No. 60/355,289, filed Feb. 8, 2002.

INT-CL: [07] G11 C 16/04

US-CL-ISSUED: 365/189.07; 365/189.04
US-CL-CURRENT: 365/189.07; 365/189.04

FIELD-OF-SEARCH: 365/189.07, 365/189.04, 365/189.08, 711/167, 711/202

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	4667337	May 1987	Fletcher	
☐	5630106	May 1997	Ishibashi	345/533
☐	5748902	May 1998	Dalton et al.	
	5953272	September 1999	Powell et al.	365/201

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☐				
☐	6046943	April 2000	Walker	
☐	6335718	January 2002	Hong et al.	
☐	2003/0041223	February 2003	Yeh et al.	711/167

ART-UNIT: 2824

PRIMARY-EXAMINER: Phung; Anh

ATTY-AGENT-FIRM: Harriman, II; J. D. Coudert Brothers LLP

ABSTRACT:

A method of writing information to a synchronous memory device by examining a present word of N bits to be written, where each bit has a high or low value. The present word is compared to a previous word also having N bits to identify the number of bit transitions from a low value to a high value or vice versa. The present bit is inverted when the number of transitions is greater than N/2. To avoid the need for having an extra bit accompany data bytes to indicate the presence or absence of inversion, the method takes advantage of a data mask pin that is normally unused during writing operations to carry the inversion bit. Non-inverted data is written directly into the memory device while inverted data is first inverted again before writing to storage locations, so that true data is stored in the memory device.

21 Claims, 8 Drawing figures

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L2: Entry 3 of 3 File: DWPI Aug 21, 2003

DERWENT-ACC-NO: 2003-731060
DERWENT-WEEK: 200369

TITLE: Memory device data transfer method for synchronous memory, involves applying data bus inversion signal on data masking pin of memory device, when next data word is to be inverted

Basic Abstract Text (1):
NOVELTY - A memory device (302) includes a data bus (DATA) and a data masking pin (302). When data word is read from the memory device, number of data signals in the next read word that are changing to complementary logic states are determined. When the determined changing states are greater than half of data signal, the next read data is inverted, and activated data bus inversion (DBI) signal is applied on the data masking pin.

Standard Title Terms (1):
MEMORY DEVICE DATA TRANSFER METHOD SYNCHRONOUS MEMORY APPLY DATA BUS INVERT SIGNAL DATA MASK PIN MEMORY DEVICE DATA WORD INVERT

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US006671212B2

(12) **United States Patent**
Macri et al.

(10) **Patent No.: US 6,671,212 B2**
(45) **Date of Patent: Dec. 30, 2003**

(54) **METHOD AND APPARATUS FOR DATA INVERSION IN MEMORY DEVICE**

(75) Inventors: **Joseph Macri**, San Francisco, CA (US); **Olga Drapkin**, Richmond Hill (CA); **Grigori Temkine**, Markham (CA); **Osamu Nagashima**, Hamura (JP)

(73) Assignee: **ATI Technologies Inc.**, Markham (CA)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 10/163,785

(22) Filed: Jun. 5, 2002

(65) **Prior Publication Data**

US 2003/0151953 A1 Aug. 14, 2003

Related U.S. Application Data

(60) Provisional application No. 60/355,289, filed on Feb. 8, 2002.

(51) Int. Cl.[7] G11C 16/04

(52) U.S. Cl. 365/189.07; 365/189.04

(58) Field of Search 365/189.07, 189.04, 365/189.08; 711/167, 202

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,667,337 A		5/1987	Fletcher	
5,630,105 A	*	5/1997	Ishibashi	345/533
5,748,902 A		5/1998	Dalton et al.	
5,953,272 A	*	9/1999	Powell et al.	365/201
6,046,943 A		4/2000	Walker	
6,335,718 B1		1/2002	Hong et al.	
2003/0041223 A1	*	2/2003	Yeh et al.	711/167

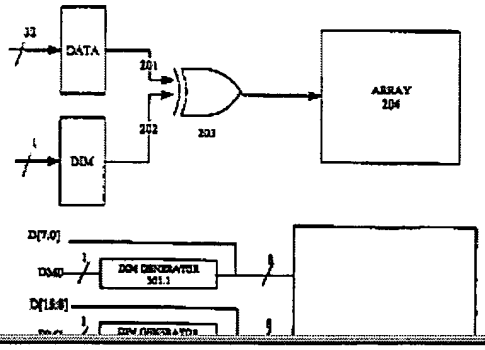
* cited by examiner

Primary Examiner—Anh Phung
(74) *Attorney, Agent, or Firm*—J. D. Harriman, II; Coudert Brothers LLP

(57) **ABSTRACT**

A method of writing information to a synchronous memory device by examining a present word of N bits to be written, where each bit has a high or low value. The present word is compared to a previous word also having N bits to identify the number of bit transitions from a low value to a high value or vice versa. The present bit is inverted when the number of transitions is greater than N/2. To avoid the need for having an extra bit accompany data bytes to indicate the presence or absence of inversion, the method takes advantage of a data mask pin that is normally unused during writing operations to carry the inversion bit. Non-inverted data is written directly into the memory device while inverted data is first inverted again before writing to storage locations, so that true data is stored in the memory device.

21 Claims, 7 Drawing Sheets



US006104662A

United States Patent [19]

Kim et al.

[11] Patent Number: 6,104,662

[45] Date of Patent: Aug. 15, 2000

[54] **DATA MASKING SYSTEMS AND METHODS FOR INTEGRATED CIRCUIT MEMORY DEVICES INCLUDING PULSE-RESPONSIVE EQUALIZERS AND PRECHARGERS**

[75] Inventors: **Jong-ryeul Kim; Kyung-woo Kang,** both of Kyungki-do, Rep. of Korea

[73] Assignee: **Samsung Electronics Co., Ltd.,** Rep. of Korea

[21] Appl. No.: **09/405,746**

[22] Filed: **Sep. 27, 1999**

[30] **Foreign Application Priority Data**

Jan. 16, 1999 [KR] Rep. of Korea 99-1160

[51] **Int. Cl.**[7] **G11C 8/00**

[52] **U.S. Cl.** **365/230.03; 365/203**

[58] **Field of Search** 365/230.03, 203, 365/204, 189.05, 191, 233

[56] **References Cited**

U.S. PATENT DOCUMENTS

5,404,338	4/1995	Murai et al.	365/233
5,517,462	5/1996	Iwamoto et al.	365/233
5,703,828	12/1997	Park et al.	365/230.03
5,844,848	12/1998	Cho	365/190

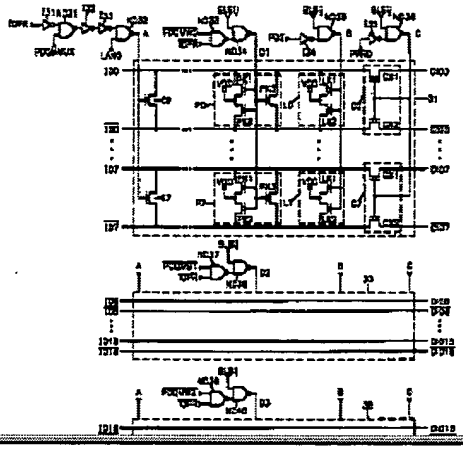
Primary Examiner—Son Mai

Attorney, Agent, or Firm—Myer Bigel Sibley & Sajovec

[57] **ABSTRACT**

Data masking is performed for an integrated circuit memory device, by generating a pulse in response to a data masking signal that is received on one of a plurality of data masking pins, equalizing a plurality of groups of input/output line pairs during the pulse and precharging the plurality of groups of input/output line pairs during the pulse. The group of input/output line pairs that correspond to the data masking signal then is precharged after the pulse in response to the data masking signal that is received on the one of the plurality of data masking pins. The input and output line drivers also preferably are deactivated during the pulse and the input and output line drivers, except for the group of input and output line drivers that correspond to the one of the plurality of data masking pins, preferably are activated after the pulse. Accordingly, the input and output line pairs that correspond to data input and output pins to be masked may be precharged during the pulse, and they may be continuously precharged after the pulse. Thus, even though the input and output line pairs may have a large resistance, they can be sufficiently precharged upon masking of write data.

10 Claims, 5 Drawing Sheets



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Search Results - Record(s) 1 through 7 of 7 returned.

☐ 1. Document ID: US 20030158981 A1

Using default format because multiple data bases are involved.

L3: Entry 1 of 7 File: PGPB Aug 21, 2003

PGPUB-DOCUMENT-NUMBER: 20030158981
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030158981 A1

TITLE: Memory bus polarity indicator system and method for reducing the affects of simultaneous switching outputs (SSO) on memory bus timing

PUBLICATION-DATE: August 21, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
LaBerge, Paul A.	Shoreview	MN	US	

US-CL-CURRENT: 710/100

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

☐ 2. Document ID: US 20030151953 A1

L3: Entry 2 of 7 File: PGPB Aug 14, 2003

PGPUB-DOCUMENT-NUMBER: 20030151953
PGPUB-FILING-TYPE: new
DOCUMENT-IDENTIFIER: US 20030151953 A1

TITLE: METHOD AND APPARATUS FOR DATA INVERSION IN MEMORY DEVICE

PUBLICATION-DATE: August 14, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Macri, Joseph	San Francisco	CA	US	
Drapkin, Olge	Richmond Hill		CA	
Temkine, Grigori	Markham		CA	
Nagashima, Osamu	Tokyo		JP	

US-CL-CURRENT: 365/189.01; 365/189.07

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 3. Document ID: US 6671212 B2

L3: Entry 3 of 7 File: USPT Dec 30, 2003

US-PAT-NO: 6671212
DOCUMENT-IDENTIFIER: US 6671212 B2

TITLE: Method and apparatus for data inversion in memory device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 4. Document ID: US 6275423 B1

L3: Entry 4 of 7 File: USPT Aug 14, 2001

US-PAT-NO: 6275423
DOCUMENT-IDENTIFIER: US 6275423 B1

TITLE: Semiconductor memory device

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 5. Document ID: US 6256248 B1

L3: Entry 5 of 7 File: USPT Jul 3, 2001

US-PAT-NO: 6256248
DOCUMENT-IDENTIFIER: US 6256248 B1
**** See image for Certificate of Correction ****

TITLE: Method and apparatus for increasing the time available for internal refresh for 1-T SRAM compatible devices

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw De

☐ 6. Document ID: US 6075740 A

L3: Entry 6 of 7 File: USPT Jun 13, 2000

US-PAT-NO: 6075740
DOCUMENT-IDENTIFIER: US 6075740 A
**** See image for Certificate of Correction ****

TITLE: Method and apparatus for increasing the time available for refresh for 1-t SRAM compatible devices

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Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

☐ 7. Document ID: US 5394366 A

L3: Entry 7 of 7 File: USPT Feb 28, 1995

US-PAT-NO: 5394366
DOCUMENT-IDENTIFIER: US 5394366 A

TITLE: Enabling data access of a unit of arbitrary number of bits of data in a semiconductor memory

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. De

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Terms	Documents
L1 and L2	7

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L1: Entry 1 of 1 File: USPT May 19, 1987

US-PAT-NO: 4667337
DOCUMENT-IDENTIFIER: US 4667337 A

TITLE: Integrated circuit having outputs configured for reduced state changes

DATE-ISSUED: May 19, 1987

INT-CL: [04] H03K 19/003, H03K 19/21

US-CL-ISSUED: 377/41; 364/707, 365/227, 307/443, 307/471
US-CL-CURRENT: 377/41; 326/21, 326/52, 326/62, 327/261, 327/403, 365/227, 713/321

FIELD-OF-SEARCH: 377/41, 307/440, 307/445, 307/362, 307/443, 307/463, 307/471, 307/473, 364/707, 365/227, 371/66

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